## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

in re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660

Group Art Unit: 2819

Filed: May 16, 2001

Examiner: D. Chang

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING MEDIUM THEREFOR

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the document listed on the attached Form PTO-1449 is hereby cited.

Respectfully submitted,

MWS:sjk

Miles & Stockbridge P.C. 1751 Pinnacle Drive, Suite 500 McLean, Virginia 22102-3833 (703) 903-9000

February 18, 2003

Mitchell W. Shapi

Reg. No. 31,568

FORM PTO-1449					Atty. Docket No.		Appln.	Appln. No.	
LIST OF DOCUMENTS CITED BY APPLICANT					XA-9472		09/8	09/855,660	
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form with next communication to Applicant.



plicant:

Yasuhisa SHIMAZAKI et al.

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XA-9472

Appln No.: Filed On:

For:

09/855,660

May 16, 2001

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND

AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING

MEDIUM THEREFOR

Attached:

Request for Continued Examination (RCE) Transmittal

w/ Check No. 9562 for \$750.00; and Request for .3-month Suspension of Action w/ Check No. 9561

for \$130.00;

Petition for Extension of Time w/ Check No. 9560

for \$110.00;

Supplemental Information Disclosure State ently

Form PTO-1449 and 1 reference.

RECEIVED IN U.S. PATENT AND TRADEMARK OFFICE ON:

ECHNOLOGY CENTER 2800

FEB 1 9 2003